AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (cancelled)

Claim 2 (currently amended): A method for determining valid bytes in an m-byte word accessed from a burst memory, comprising:

receiving a plurality of access parameters; and

generating an m-bit enable word from the access parameters and a value of m, said m-bit enable word including at least one valid bit corresponding to at least one valid byte in the m-byte word further comprising making a client request to memory, wherein the access parameters from which the m-bit enable word is generated include:

a first address; and

a byte count value indicating a number of bytes in said client request to memory.

Claim 3 (original): The method of claim 2, wherein generating the m-bit enable word comprises:

truncating a portion of the first address to produce an n-bit word;

generating an enable value from the n-bit word, the byte count value, and the m value;

generating an m-bit pre-shifted enable word from the enable value and the m value; and

shifting the bits in the m-bit pre-shifted enable word by a value of the n-bit word.

Claim 4 (original): The method of claim 3, wherein the n value equals a base two logarithm of the m value minus one, and said n-bit word comprises a plurality of bits between and including a least significant bit and a bit in position n in the first address.

Claim 5 (original): The method of claim 3, further comprising:

in response to the byte count value and the enable value, determining whether an access to memory satisfies a client request which generated the access.

Claim 6 (original): The method of claim 3, further comprising:

generating a second address for a subsequent access to memory from the first address and the enable value.

Claim 7 (previously presented): The method of claim 2, wherein the value of m is thirty-two.

Claim 8 (cancelled)

Claim 9 (currently amended): A memory controller comprising:

a data input to receive a plurality of access parameters from a client device and an access bytes value indicating a number of bytes in a burst word from a memory device; and

an enable circuit to determine at least one valid byte in the burst word in response to the plurality of access parameters and the access bytes value,

wherein the plurality of access parameters in response to which the at least one valid byte in the burst word is determined include:

a first address; and

a byte count value indicating a number of bytes in a client request to memory.

Claim 10 (original): The memory controller of claim 9, further comprising:

an enable word generator to generate an enable word including at least one valid bit corresponding to the at least one valid byte in the burst word.

Claim 11 (original): The memory controller of claim 10, wherein the burst word comprises an m-byte word and the enable word comprises an m-bit word.

Claim 12 (cancelled)

Claim 13 (cancelled)

Claim 14 (currently amended): A system, comprising:

a memory device comprising a plurality of memory elements, each memory element having an associated address;

a client device;

a bus to pass data between the memory device and the client device; and

a memory controller to control an access by the client device to an m-byte burst word in the memory device over the bus, said memory controller operating to receive a plurality of access parameters from the client device and determine at least one valid byte in the m-byte word in response to the plurality of access parameters and a value of m

wherein the memory controller comprises an enable word generator to generate an enable word including at least one valid bit corresponding to the at least one valid byte in the burst word and

wherein the memory controller is operative to receive a client request to memory, and wherein the plurality of access parameters, from which the at least one valid byte is determined, include:

a first address; and

a byte count value indicating a number of bytes in said client request to memory.

Claim 15 (original): The system of claim 14, wherein the memory controller is operative to determine a second address for a subsequent access for the plurality of access parameters.

Claim 16 (original): The system of claim 15, wherein the client is operative to store the second address.

Claim 17 (previously presented): The system of claim 14, wherein the memory device is a burst memory device.

Claim 18 (previously presented): The system of claim 14, wherein the memory controller is operative to determine whether the access is a last access required to satisfy a client request.

Claim 19 (previously presented): The system of claim 14, wherein the bus comprises a read bus and a write bus.

Claim 20 (cancelled)

Claim 21 (currently amended): Apparatus, including instructions residing on a machine-readable medium, for determining valid bytes in an m-byte word accessed from a burst memory, said instructions causing the machine to:

receive a plurality of access parameters; and

generate an m-bit enable word from the access parameters and the m value, said m-bit enable word including at least one valid bit corresponding to at least one valid byte in the m-byte word

wherein the access parameters, from which the m-bit enable word is generated, include:

a first address; and

a byte count value indicating a number of bytes in a client request to memory.

Claim 22 (original): The apparatus of claim 21, wherein the instructions to generate the m-bit enable word comprise instructions causing the machine to:

truncate a portion of the first address to produce an n-bit word;

generate an enable value from the n-bit word, the byte count value, and the m value;

generate an m-bit pre-shifted enable word from the enable value and the m value; and

shift the bits in the m-bit pre-shifted enable word by a value of the n-bit word.

Claim 23 (original): The apparatus of claim 22, wherein the n value equals a base two logarithm of the m value minus one, and said n-bit word comprises a plurality of bits between and including a least significant bit and a bit in position n in the first address.

Claim 24 (original): The apparatus of claim 22, further comprising instructions that cause the machine to:

determine whether an access to memory satisfies a client request in response to the byte count value and the enable value.

Claim 25 (original): The apparatus of claim 22, further comprising instructions that cause the machine to:

generate a second address for a subsequent access to memory from the first address and the enable value.

Claim 26 (previously presented): The apparatus of claim 21, wherein the value of m is thirty-two.